We Claim:

1. A bridge apparatus, comprising:

a first bus adapted to facilitate data transfer;

a second bus adapted to facilitate data transfer; and

a bridge coupling the first bus to the second bus, the bridge adapted to perform memory read, memory read line, and memory read multiple commands from the first bus to the second bus, wherein the bridge responds to the memory read multiple command differently than either the memory read or the memory read line command.

2. The bridge apparatus of claim 1 wherein the memory read multiple command prefetches more data than the memory read command.

3. The bridge apparatus of claim 1 wherein the amount of data prefetched by the memory read multiple command is selectively variable in size.

4. The bridge apparatus of claim 1 wherein the memory read multiple command prefetches more data than the memory read line command.

5. The bridge apparatus of claim 1 wherein second bus has cache memory, wherein the bridge apparatus is adapted to perform memory read multiple command with the cache memory.

6. The bridge apparatus of claim 1 wherein second bus has RAM memory, wherein the bridge apparatus is adapted to perform memory read multiple command with the RAM memory.

7. The bridge apparatus of claim 1 wherein the bridge has a prefetch buffer, wherein the prefetch buffer is adapted to be flushed after a memory read multiple command by the first bus.

8. The bridge apparatus of claim 1 wherein the memory read multiple command utilizes at least 32 Dwords.

9. The bridge apparatus of claim 1 wherein the memory read multiple command utilizes at least 64 Dwords.

10. The bridge apparatus of claim 1 wherein a prefetch size of a memory read multiple command is at least four times as large as the size of a memory read or memory read line command.

11. The bridge apparatus of claim 1 wherein the first bus is a PCI bus.

12. The bridge apparatus of claim 1 wherein the second bus is a PCI bus.

13. The bridge apparatus of claim 1 wherein the second bus is adapted to support a SCSI disk controller.

14. The bridge apparatus of claim 1 wherein the second bus is a PCI bus.

15. A controller apparatus, comprising:

a first bus adapted to facilitate data transfer;

a second bus adapted to facilitate data transfer; and

a controller coupling the first bus to the second bus, the controller adapted to perform memory read, memory read line, and memory read multiple commands from the first bus to the second bus.

16. A method of operating a bridge coupled between a first bus and a second bus, comprising:

initiating a read multiple command on the first bus;

the bridge passing the read multiple command to a target on the second bus, wherein the bridge also supports a memory read and a memory read line command; and

the bridge treating the read multiple command differently than the memory read line command.

17. The method of claim 16 wherein the bridge prefetches more data in response to the memory read multiple command than that prefetched in response to a memory read command.

19. A controller adapted to prefetch data via a first bus from a target on a second bus, comprising a circuit adapted to respond to a memory read multiple command and a memory read line command, whereby the circuit prefetches more data from the target in response to the memory read multiple command than the memory read command.

20. The controller as specified in claim 19 wherein the circuit prefetches more data from the target in response to the memory read multiple command than the memory read line command.